AMENDMENTS TO THE CLAIMS

Claim 1 (original): A semiconductor memory device comprising:

a plurality of memory cells, each of which is capable of storing N-level data (N represents a natural number of 2 or greater) and being reprogrammed;

a plurality of monitor cells that separately store individual data values of the N-level data by using the same scheme as that used by the memory cells;

sensing means for sensing whether a physical quantity of the monitor cell which corresponds to the data value stored in the monitor cell is within a preset range; and

verification means for verifying whether the physical quantity of the memory cell which corresponds to the data value stored in the memory cell is within the preset range when the sensing means has sensed that the physical quantity of the monitor cell is out of the preset range.

Claim 2 (currently amended): The semiconductor memory device according to claim 1, wherein the monitor cells include at least a first monitor cell [[or]] and a second monitor cell, the first monitor cell monitoring deteriorations caused in read operations for data retention states of the memory cells, and the second monitor ~~cells~~ cell monitoring time-dependent deteriorations of the data retention states of the memory cells.

Claim 3 (currently amended): The semiconductor memory device according to claim 2, wherein the semiconductor memory device is configured such that stresses influencing the deteriorations of the data retention states, which stresses occur with the read operations, on the first monitor ~~cells~~ cell are greater than the stresses on the memory cells which are monitoring targets of the first monitor ~~cells~~ cell.

Claim 4 (original): The semiconductor memory device according to claim 2, wherein the semiconductor memory device is configured such that each time a read operation takes place for the memory cell which is a monitoring target of the first monitor cell, at least one read operation is executed on the first monitor cell.

Claim 5 (currently amended): The semiconductor memory device according to claim 2, wherein the semiconductor memory device is configured such that stresses influencing deteriorations of data retention states on the second monitor ~~cells~~ cell in state not directly receiving a read operation, a program operation, and an erase operation is greater than the stresses on the memory cells which are monitoring targets of the second monitor ~~cells~~ cell.

Claim 6 (currently amended): The semiconductor memory device according to claim 2, wherein the plurality of monitor cells are disposed between the plurality of the memory cells, which are the monitoring targets of the second monitor ~~cells~~ cell, and load circuits that supply voltages required for the read operation to the memory cells.

Claim 7 (original): The semiconductor memory device according to claim 1, further comprising a timing generation circuit that generates a synchronizing signal for the sensing means to execute sensing of the physical quantity of the monitor cell with a predetermined timing.

Claim 8 (original): The semiconductor memory device according to claim 1, further comprising correction means for correcting the physical quantity of the memory cell to be within the preset range when the verification means has verified the physical quantity of the memory cell to be out of the preset range.

Claim 9 (original): The semiconductor memory device according to claim 8, wherein the correction means corrects the physical quantity by executing at least programming or erasure on the memory cell which is a correction target.

Claim 10 (original): The semiconductor memory device according to claim 1, wherein the memory cell is configured to comprise a selection transistor and a nonvolatile variable resistor element permitting electrical resistance to be varied by electrical stresses and retaining the varied electrical resistance even after the electrical stresses have been relieved.

Claim 11 (original): The semiconductor memory device according to claim 10, wherein in the nonvolatile variable resistor element, an oxide having a perovskite structure containing manganese is formed between electrodes.

Claim 12 (original): A correction method for correcting data stored in memory cells, each of which is capable of storing N-level data (N represents a natural number of 2 or greater) and being reprogrammed, the correction method comprising:

using a plurality of monitor cells that separately store individual data values of the N-level data by using the same scheme as that used for the memory cells;

sensing whether a physical quantity of the monitor cell which corresponds to the data value stored in the monitor cell is within a preset range;

verifying whether the physical quantity of the memory cell which corresponds to the data value stored in the memory cell is within the preset range when the sensing means has sensed that the physical quantity of the monitor cell is out of the preset range; and

correcting the physical quantity of the memory cell to be within the preset range when the physical quantity of the memory cell has been verified to be out of the preset range.

Claim 13 (original): The correction method according to claim 12, wherein the monitor cells include at least a first monitor cell or a second monitor cell, the first monitor cell monitoring deteriorations caused in read operations for data retention states of the memory cells, and the second monitor cell monitoring time-dependent deteriorations of the data retention states of the memory cells.

Claim 14 (original): The correction method according to claim 12, wherein the step of sensing whether the physical quantity of the monitor cell is within the preset range is performed with timing based on a synchronizing signal generated by a timing generation circuit provided to generate synchronizing signals that are used to execute sensing of physical quantities of the monitor cells with predetermined timings.

Claim 15 (original): The correction method according to claim 12, wherein the memory cell is configured to comprise a selection transistor and a nonvolatile variable resistor element permitting electrical resistance to be varied by electrical stresses and retaining the varied electrical resistance even after the electrical stresses have been relieved.

Claim 16 (original): The correction method according to claim 15, wherein in the nonvolatile variable resistor element, an oxide having a perovskite structure containing manganese is formed between electrodes.